REMARKS/ARGUMENTS

Claims 1-11 are pending in the application.

Claim 11 has been cancelled.

Claims 1-11 are rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response to the §112 rejection, Applicant has amended FIG. 1 to provide clarification for the dimensional terms used throughout the Specification. Such terms include length, depth, thickness, *et al.* Furthermore, annotations indicating parts of the inventive structure have been included to facilitate the discussion presented. Parts of the Specification were amended to clarify any ambiguities with respect to the §112 rejections, as well. These changes are supported by the Specification and contain no new matter. Applicant believes that these amendments overcome the §112 rejections and request that they be withdrawn.

The Office action objects to the disclosure for lacking section headings under 37 CFR 1.77(b). Applicants respectfully traverse this objection. Applicants prefer not to add section headings, for consistency with the parent application. Such section headings are not statutorily required for filing a non-provisional patent application under 35 USC 111(a), but per 37 CFR 1.51(d) are only guidelines that are suggested for Applicants' use. They are not mandatory, and in fact when Rule 77 was amended in 1996 (61 FR 42790, Aug. 19, 1996), Bruce A. Lehman, Assistant Secretary of Commerce and Commissioner of Patents and Trademarks, states in the Official Gazette:

> **"Section 1.77 is permissive rather than mandatory. ... 1.77 merely expresses the Office's preference for the arrangement of the application elements. The Office may advise an applicant that the application does not comply with the format set forth in 1.77, and suggest this format for the applicant's consideration; however, the Office will not require any application to comply with the format set forth in 1.77."**
> *Miscellaneous Changes in Patent Practice, Response to comments 17 and 18 (Official Gazette, August 13, 1996) [Docket No: 950620162-6014-02] RIN 0651-AA75.*

Applicants respectfully request that the Examiner withdraw his objections.

Claim 1 has been amended to better clarify the feature of "a liner of a first insulating material."

Claims 1-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Sugiura et al.* (US 6,150,686). Applicant respectfully traverses the rejection.

Argument for Claims 1-7

Sugiura "relates to a semiconductor integrated circuit device and, more particularly, to a dynamic semiconductor memory device using a trench capacitor as a capacitor element constituting a memory cell. The memory cell of a dynamic semiconductor memory device (to be referred to as a DRAM hereinafter) is made up of a capacitor and a transfer insulated gate transistor. To increase the integration degree of the DRAM, capacitors with larger capacitance values are desirably formed in a smaller area. One means for realizing such a structure is a trench capacitor obtained by constituting a capacitor using a trench formed in a silicon substrate (col. 1, lines 5-10)." Of trench capacitors, a BEST (BuriEd STrap) cell receives a great deal of attention as a capacitor which can cope with a mass DRAM in the Gbit (Gigabit) class. . . (col. 1, lines 18-20) The trench capacitor of the BEST cell is obtained by forming an n-buried well in a p-silicon substrate, forming a trench to reach the n-well, and forming a storage electrode in this trench. The n-buried well functions as a plate electrode (col. 1, lines 27-30)."

In contrast, Applicant's claimed features are unlike the memory structure of *Sugiura*. Applicant's invention is "It is an object of the present invention to provide an improved trench isolation structure of the indicated kind, which provides favourable parasitic capacitance values while ensuring at the same time good insulating properties and low thermally induced stress, when used in a semiconductor device assembly. In this way, a smaller minimum device assembly dimension becomes possible (Specification, page 2, lines 27-31)." Furthermore, "said object is achieved by a trench isolation structure according to the invention, which is characterized in that at least in a first part of the trench groove which is surrounded by the buried layer, the thickness is larger than the thickness in a second part of the trench groove which is located below the first part. (Specification, page 2, lines 33-34; page 3, lines 1-2)."

Applicant asserts that one skilled in the art would not select *Sugiura* in that he does not suggest or teach Applicant's invention. Figure 2 of the reference is a "sectional view showing the dynamic memory cell (col. 3, lines 58-59)." Applicant addresses a long-felt need, "with the known trench isolation structures is that they do not provide at the same time low parasitic capacitance values and minimum stress generated due to mismatch of thermal expansion coefficients. This limits the integration in a full BiCMOS process. It specifically limits the reduction of collector-collector spacing or minimum device dimensions in general (Specification, page 2, lines 20-25)." *Sigiura*, on the other,

is directed to DRAM active structures—not Applicant's claimed trench isolation structures.

Consequently, Applicant's claimed features are patentable over the cited reference. Applicant requests that the rejections for claims 1-7 be withdrawn.

Argument for Claims 8-10

In that Applicant has addressed the §112 issues with respect to these claims and that no other rejection had been raised in the Office Action, Applicant respectfully asserts that claims 8-10 are allowable.

Conclusion

Applicant believes he has addressed the Examiner's concerns. Applicant requests a timely Notice of Allowance.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 50-4019.

Respectfully submitted,

Date: 07-DEC-2006

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